WHEN DO EXTRA MAJORITY GATES HELP? POLYLOG(N) MAJORITY GATES ARE EQUIVALENT TO ONE

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Abstract. Suppose that a Boolean function f is computed by a constant depth circuit with 2^m AND-, OR-, and NOT-gates—and m majority-gates. We prove that f is computed by a constant depth circuit with $2^{m^{O(1)}}$ AND-, OR-, and NOT-gates—and a single majority-gate, which is at the root.

One consequence is that if a Boolean function f is computed by an AC^0 circuit plus polylog majority-gates, then f is computed by a probabilistic perceptron having polylog order. Another consequence is that if f agrees with the parity function on three-fourths of all inputs, then f cannot be computed by a constant depth circuit with $2^{n^{o(1)}}$ AND-, OR-, and NOT-gates, and $n^{o(1)}$ majority-gates.

Key words. Majority-gate; threshold-gate; symmetric gate; circuit; parity.

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1. Introduction

One of the goals of complexity theory is to find ways to reduce the use of one resource. Typically this entails a modest increase in some other resources.

Recently, quasipolynomial size circuits have been the setting for unexpected resource tradeoffs (Allender 1989, Allender & Hertrampf 1994, Yao 1990, Beigel & Tarui 1994, Tarui 1993, and Beigel *et al.* 1991). In this paper we show how to reduce the number of majority-gates in many kinds of quasipolynomial size circuits from polylog to 1.

For example, consider constant depth quasipolynomial size circuits that consist of AND-, OR-, NOT-, and majority-gates. We show how to reduce the number of majority-gates from m to 1, while increasing the number of other gates by $2^{m \operatorname{polylog} n}$ and increasing the depth by 2. As a corollary we convert such circuits to probabilistic perceptrons having small order. As another corollary, we unify the lower bounds of Aspnes *et al.* (1991), Yao (1985), Hastad (1989), and Siu *et al.* (1993) for computing parity with constant depth circuits, proving that if a constant depth circuit consisting of AND-, OR-, NOT-, and majority-gates computes parity correctly on three-fourths of all inputs, then the circuit must have exponential size or a polynomial number of majority-gates.

Our result is an exponential improvement on the bounds of Beigel *et al.* (1994). The proof uses the low-degree polynomials developed in that paper and an observation of Fortnow & Reingold (1991) in a nontrivial way.

We also show how to reduce the number of symmetric gates in many kinds of quasipolynomial size circuits from $O(\log\log n)$ to 1. Consider constant depth quasipolynomial size circuits that consist of AND-, OR-, NOT-, and MOD_k-gates and symmetric gates. We show how to reduce the number of symmetric gates from m to 1, while increasing the number of other gates by $2^{2^m \operatorname{polylog} n}$ and increasing the depth by 1. The proof uses base-B representation in the same way as Papadimitriou & Zachos (1983). As a corollary we extend results of Yao (1990) and Beigel & Tarui (1994) on ACC, showing that any function computed by a constant depth, quasipolynomial size circuit consisting of AND-, OR-, NOT-, and MOD_k-gates and $O(\log\log n)$ symmetric gates is in fact computed by a depth 2, quasipolynomial size circuit with a symmetric gate at the root and AND-gates having polylog fanin at the bottom level.

Our results are for circuits with a single Boolean output gate. Amir *et al.* (1990) obtained contrasting results for circuits with multiple output gates. They proved in a very general setting that $m+1$ majority-gates permit such circuits to compute more functions than only m majority-gates; in fact, their result holds not only for threshold-gates but for any nontrivial gate.

2. Representing Boolean functions

Boolean values are often represented as elements of $\{0,1\}$, 0 denoting false, and 1 denoting true. They can also be represented as elements of $\{-1,1\}$, -1 denoting false and 1 denoting true. Real polynomials or rational functions in either representation can be converted to the other without affecting the degree.

A majority-gate outputs true if more than half of the inputs are true. By standard techniques, we will assume that it is never the case that exactly half of the inputs to a majority-gate are true.

In the first representation, the majority function is

$$\mathrm{MAJ}(x_1,\ldots,x_n) = \begin{cases} 1 & \text{if } \sum x_i > \frac{1}{2}n, \\ 0 & \text{if } \sum x_i < \frac{1}{2}n. \end{cases}$$

In the second representation,

$$\mathrm{MAJ}(x_1,\ldots,x_n) = \mathrm{sgn}(\textstyle\sum x_i),$$

where $\mathrm{sgn}(x)$ denotes the signum function (-1 if $x < 0$, 1 if $x > 0$, and 0 if $x = 0$).

A threshold-gate computes a weighted sum of the inputs and tests whether the sum is greater than a threshold. In circuits, a threshold-gate with integer weights can be simulated by a majority-gate, because we can use parallel wires to simulate weights. Thus our results for circuits with majority-gates hold as well for circuits with threshold-gates having small integral weights. The results for threshold circuits will not be stated explicitly.

3. Approximations

Rational approximations were developed by Newman (1964). Low-degree rational approximations are an important tool, which was applied to threshold circuit lower bounds by Paturi & Saks (1994). In order to prove upper bounds, Beigel *et al.* (1994) observed that small integral coefficients are also important.

DEFINITION 3.1. *A real-valued function* $g(x_1,\ldots,x_n)$ approximates *a function* $f(x_1,\ldots,x_n)$ *with error* ϵ *if for all* $x_1,\ldots,x_n$ *in the domain of* f, $|g(x_1,\ldots,x_n) - f(x_1,\ldots,x_n)| \le \epsilon$.

LEMMA 3.2 (BEIGEL *et al.* 1994). $\mathrm{MAJ}(x_1,\ldots,x_n)$ *can be approximated with error* ϵ *by a rational function* $g(x_1,\ldots,x_n)$ *having degree* $O(\log n \log(1/\epsilon))$ *and integer coefficients bounded by* $2^{O(\log^2 n \log(1/\epsilon))}$.

Definition 3.3.

- *The* norm *of a polynomial is the sum of the absolute values of its coefficients.*
- *The* norm *of a rational function is the norm of its numerator plus the norm of its denominator.*

This definition of norm will be robust enough for our purposes because changing between the $\{0,1\}$ representation of Boolean values and the $\{-1,1\}$ representation changes the norm of a degree d rational function by a factor of only $2^{O(d)}$.

Note that the value of a polynomial over $\{0,1\}^k$ or over $\{-1,1\}^k$ is bounded by its norm. We need the following easy corollary to Lemma 3.2.

Lemma 3.4. *Let n be any natural number.* $\mathrm{MAJ}(x_1,\ldots,x_n)$ *can be approximated with error ϵ by a rational function $g(x_1,\ldots,x_n)$ having norm* $2^{O(\log^2 n \log(1/\epsilon))}$.

Proof. The number of monomials in a polynomial with n variables and degree d is $\binom{n+d}{d}$. Therefore the numerator and the denominator of the rational function in Lemma 3.2 contain $n^{O(\log n \log(1/\epsilon))}$ monomials, which is $2^{O(\log^2 n \log(1/\epsilon))}$. The coefficients are also $2^{O(\log^2 n \log(1/\epsilon))}$. $\square$

4. Eliminating majority-gates

Let G be any set of gates that includes unbounded fanin AND-gates. Let $\mathrm{ThreshC}_G$(depth d, size s, majorities m) denote the class of circuits consisting of gates in G and majority-gates with depth d, size s, and m majority-gates. Let C_G(depth d, size s) denote $\mathrm{ThreshC}_G$(depth d, size s, majorities 0).

Theorem 4.1. *Suppose that f is in* $\mathrm{ThreshC}_G$(depth d, size s, majorities m). *Then f is in* $\mathrm{ThreshC}_G$(depth d+2, size $2^{m(O(\log s))^{2d+1}}$, majorities 1), *where the majority-gate is at the root.*

Taking $G = \{\text{AND}, \text{OR}, \text{NOT}\}$ and $d = O(1)$, this exponentially improves the size bound of Beigel *et al.* (1994).

A perceptron is a depth-2 circuit with a threshold-gate at the root and AND-gates at the other level. The *order* of a perceptron is the maximum fanin of its AND-gates. The *weight* of a perceptron is the maximum absolute value of its threshold-gate's weights. A *probabilistic perceptron* has ordinary Boolean inputs $x_1, \ldots, x_n$ and random Boolean inputs $r_1, \ldots, r_m$. A probabilistic perceptron computes a Boolean function f if, for all $x_1, \ldots, x_n$, for at least three-fourths of all $r_1, \ldots, r_m$, the circuit's output is equal to $f(x_1, \ldots, x_n)$. Let $G = \{\text{AND}, \text{OR}, \text{NOT}\}$; Tarui (1993) and Beigel *et al.* (1991) proved that every Boolean function computed by a ThreshC_G(depth d, size s, majorities 1) circuit where the majority-gate is at the root is, in fact, computed by a probabilistic perceptron having order $(\log s)^{O(d)}$ and weight $2^{(\log s)^{O(d)}}$. The following extensions of their result are immediate.

Corollary 4.2. *Let* $G = \{\text{AND}, \text{OR}, \text{NOT}\}$. *Every function in* ThreshC_G(depth d, size s, majorities m) *is computable by a probabilistic perceptron having order* $(m \log s)^{O(d)}$ *and weight* $2^{(m \log s)^{O(d)}}$.

Corollary 4.3. *Let* $G = \{\text{AND}, \text{OR}, \text{NOT}\}$. *Every function in* ThreshC_G(depth $O(1)$, size quasipolynomial, majorities polylog) *is computable by a probabilistic perceptron having polylog order and quasipolynomial weight.*

Let $G = \{\text{AND}, \text{OR}, \text{NOT}\}$. Yao (1985) and Hastad (1989) proved that C_G(depth $O(1)$, size $2^{n^{o(1)}}$) circuits cannot compute parity correctly on all inputs. This was improved by Cai (1989) and Babai (1987), who showed that such circuits cannot compute parity correctly on even three-fourths of all inputs. This was further improved by Aspnes *et al.* (1991), who showed that ThreshC_G(depth $O(1)$, size $2^{n^{o(1)}}$, majorities 1) circuits where the majority gate is at the root cannot compute parity correctly on three-fourths of all inputs. Siu *et al.* (1993) proved that $\text{ThreshC}_\emptyset$(depth $O(1)$, size $n^{o(1)}$, majorities $n^{o(1)}$) circuits cannot compute parity correctly on all inputs. By combining Theorem 4.1 with the result of Aspnes *et al.* (1991) we unify the bounds just stated.

Corollary 4.4. *Let* $G = \{\text{AND}, \text{OR}, \text{NOT}\}$. *If f agrees with parity on three-fourths of all inputs in* $\{0,1\}^n$ *then f is not in* ThreshC_G(depth d, size $2^{n^{o(1/d^2)}}$, majorities $n^{o(1/d)}$).

For comparison, parity can be computed exactly by circuits with $O(n^{O(1/d)})$ majority-gates alone (Siu *et al.* 1993) or with $2^{n^{O(1/d)}}$ AND-, OR-, and NOT-gates alone (Håstad 1986). In Corollary 4.4, the special case $d = O(1)$ is notable.

COROLLARY 4.5. *Constant depth circuits consisting of AND-, OR-, NOT-, and majority-gates require either exponential size or a polynomial number of majority-gates in order to compute parity correctly on three-fourths of all inputs.*

PROOF OF THEOREM 4.1. It will be convenient to assume that f's arguments are in $\{0,1\}$ and that f's result is in $\{-1,1\}$. Let $f : \{0,1\}^n \to \{-1,1\}$ belong to $\mathrm{ThreshC}_G$(depth d, size s, majorities m). We will show that $f = \mathrm{sgn}(p(f_1,\ldots,f_\ell))$ where p has norm $2^{m(O(\log s))^{2d+1}}$ and $f_1,\ldots,f_\ell$ belong to C_G(depth d, size s). (In fact if we view the original circuit as a DAG, $f_1,\ldots,f_\ell$ are some of its subgraphs.) That proves the theorem, because products can be computed by AND-gates when inputs are represented in $\{0,1\}$.

Let $\mathrm{ThreshC}_G$(depth d, size s, majorities m, level k) denote the class of $\mathrm{ThreshC}_G$(depth d, size s, majorities m) circuits with majority-gates on only levels 0 through k, where level 0 is the root. If f is computed by a $\mathrm{ThreshC}_G$(depth d, size s, majorities m, level k) circuit we will construct p and $f_1,\ldots,f_\ell$ such that $f = \mathrm{sgn}(p(f_1,\ldots,f_\ell))$, p is a polynomial whose norm is bounded by some function $N_p(k)$, and $f_1,\ldots,f_\ell$ belong to C_G(depth d, size s). We will find a recurrence for $N_p(k)$, and show that $N_p(k) = 2^{m(O(\log s))^{2k+1}}$. The theorem follows from that bound, taking $k = d$.

We use -1 to represent false and 1 to represent true. Consider a function f computed by a circuit C with majority-gates only on levels 0 through k. Let $g_1,\ldots,g_t$, where $t \le m$, denote the majority-gates on level k. If $(b_1,\ldots,b_i) \in \{-1,1\}^t$, we let $f_{b_1,\ldots,b_t}$ be the function computed by the circuit obtained from C when we replace g_i by the constant b_i for all i, and we let $c_{b_1,\ldots,b_t}$ equal 1 if the output of g_i is b_i for all i and 0 otherwise. Then

$$f = \sum_{(b_1,\ldots,b_t)\in\{-1,1\}^t} f_{b_1,\ldots,b_t} c_{b_1,\ldots,b_t}.$$

The function $f_{b_1,\ldots,b_t}$ is the sign of a polynomial p of C_G(depth d, size s) functions, where the norm of p is bounded by $N_p(k-1)$. The function $c_{b_1,\ldots,b_t}$ is the product of exactly t factors, each of which is either a majority or its complement. Let $\epsilon = 1/(m(2^m N_p(k-1)+1))$. Each majority has at most s

inputs, so it can be approximated within error ϵ by a rational function whose norm is $2^{O((\log^2 s)(m+\log N_p(k-1)))}$, by Lemma 3.4.

If a majority-gate is approximated within ϵ by the rational function r, then its complement is approximated within ϵ by the rational function $1-r$, which has the same denominator as r. If r is as in the previous paragraph, then the norm of $1-r$ is also $2^{O((\log^2 s)(m+\log N_p(k-1)))}$.

We approximate the function $c_{b_1,\ldots,b_k}$ by the product of the rational functions that approximate the corresponding majorities or their complements. The error is at most $(1+\epsilon)^t - 1 \leq (1+\epsilon)^m - 1$. Furthermore the denominator is the same for each term because r and $1-r$ have the same denominator. Call the approximation $\hat{c}_{b_1,\ldots,b_k}$.

Then the function f is approximated by taking the sum of the 2^m terms of the form $f_{b_1,\ldots,b_t}\hat{c}_{b_1,\ldots,b_t}$. Since $|f_{b_1,\ldots,b_t}|$ is bounded by $N_p(k-1)$, the error in approximating f is bounded by $2^m N_p(k-1)((1+\epsilon)^m - 1)$, which is less than 1 by Lemma 4.6 (proved below) with $N = N_p(k-1)$, so the approximation has the same sign as f.

Recall that all the rational functions used in the approximation have the same denominator. We obtain a polynomial that has the same sign as f by multiplying by the square of that common denominator. If N_r bounds the norm of the rational functions and $N_p(k-1)$ bounds the norm of the polynomials p that computes $f_{b_1,\ldots,b_t}$ then $2^m N_p(k-1)N_r^2$ bounds the norm of the resulting polynomial, so

$$N_p(k) \leq 2^m N_p(k-1) 2^{O((\log^2 s)(m+\log N_p(k-1)))}.$$

Furthermore, we have $N_p(0) < s$. An easy induction shows that

$$N_p(k) = 2^{(m+\log s)(O(\log s))^{2k}} = 2^{m(O(\log s))^{2k+1}}. \ \Box$$

Lemma 4.6. *Let* $\epsilon = 1/(m(2^m N + 1))$. *Then* $2^m N((1+\epsilon)^m - 1) < 1$.

Proof. For all real y, $1 + y \leq e^y$, with equality holding iff $y = 0$. By inverting that inequality and letting $y = -1/(1+x)$ where $x > 0$, we obtain

$$1 + 1/x > e^{\frac{1}{1+x}} = (e^{\frac{1}{m(1+x)}})^m > (1 + \frac{1}{m(x+1)})^m.$$

Letting $x = 2^m N$, we have

$$2^m N((1+\epsilon)^m - 1) < 2^m N(1 + 2^{-m} N^{-1} - 1) = 1,$$

as claimed. $\Box$

5. Eliminating Symmetric Gates

By applying some simple techniques developed by Papadimitriou & Zachos (1983) in the study of #P, we will show how to reduce the number of symmetric gates in circuits to 1. Let SymmC_G(depth d, size s, symmetrics m) denote the class of circuits consisting of gates in G and symmetric gates with depth d, size s, and m symmetric gates. (In this section G need not contain unbounded fanin AND-gates.)

THEOREM 5.1. *Suppose that f is in* SymmC_G(depth d, size s, symmetrics m). *Then f is in* SymmC_G(depth $d+1$, size s^{2^m+1}, symmetrics 1), *where the symmetric gate is at the root.*

PROOF. In this proof, we write "subcircuit" to mean a subcircuit containing only gates in G; subcircuits may have more than one output. Consider any circuit C with m symmetric gates, $g_1, \ldots, g_m$ where the depth of g_{i-1} is at least as great as the depth of g_i for $i = 2, \ldots, m$. Trying all possible output values for $g_1, \ldots, g_{i-1}$ we find that g_i computes a symmetric function of one of 2^{i-1} subcircuits of C. Doing so for all i, we see that it is sufficient to evaluate $2^m - 1$ symmetric functions of subcircuits of C and to evaluate a subcircuit of C in the case that there is not a symmetric gate at the root. A fortiori, it suffices to evaluate 2^m symmetric functions of subcircuits of C. Let $M = 2^m$, and let $x_0, \ldots, x_{M-1}$ respectively denote the sum of the inputs to each of those symmetric functions. All of these numbers can be encoded into a single number, $X = \sum_{i=0}^{M-1} x_i B^i$, where B is any number larger than each of the x_i's; taking $B = s$ suffices. The number X, and hence the function f, may be computed by a single symmetric gate whose inputs are $(B^M - 1)/(B - 1)$ subcircuits of C. The size of the resulting circuit is at most

$$s(B^M - 1)/(B - 1) = s(s^{2^m} - 1)/(s - 1) < s^{2^m+1}. \quad \square$$

ACC is the class of Boolean functions computed by constant-depth polynomial-size circuits consisting of AND-, OR-, NOT-, and MOD_k-gates for some positive integer k (the number k may depend on the function but not on the input length). Yao (1990) proved that every function in ACC is computable by a depth-2 quasipolynomial-size probabilistic circuit with a symmetric gate at the root and polylog-fanin AND-gates at the leaves. Let

$G = \{\mathrm{AND}, \mathrm{OR}, \mathrm{NOT}, \mathrm{MOD}_k\}$; Beigel & Tarui (1994) improved Yao's result, showing that every function in SymmC_G(depth d, size s, symmetrics 1) where the symmetric gate is at the root is, in fact, computed by a depth-2 $2^{(\log s)^{2^{O(d)}}}$-size deterministic circuit with a symmetric gate at the root and $(\log s)^{2^{O(d)}}$-fanin AND-gates at the leaves. By combining Theorem 5.1 with Beigel and Tarui's result, we obtain the following extension.

COROLLARY 5.2. *Let* $G = \{\mathrm{AND}, \mathrm{OR}, \mathrm{NOT}, \mathrm{MOD}_k\}$. *Then every function in* SymmC_G(depth d, size s, symmetrics m) *is computable by a depth-*2 $2^{(2^m \log s)^{2^{O(d)}}}$*-size deterministic circuit with a symmetric gate at the root and* $(2^m \log s)^{2^{O(d)}}$*-fanin AND-gates at the leaves.*

The following special case is notable.

COROLLARY 5.3. *Let* $G = \{\mathrm{AND}, \mathrm{OR}, \mathrm{NOT}, \mathrm{MOD}_k\}$. *Then every function in* SymmC_G(depth $O(1)$, size quasipolynomial, symmetrics $O(\log\log n)$) *is computable by a depth-*2 *quasipolynomial-size circuit with a symmetric gate at the root and polylog-fanin AND-gates at the leaves.*

6. Extensions

When we eliminate majority-gates, it is notable that unbounded-fanin AND-gates are not always required. The fanin of the AND-gates at the second level of the simulating circuits is bounded by the degree of the polynomial associated with the construction. Furthermore, we have noted that the subcircuits which feed into those AND-gates are subgraphs of the original circuit. Our size bounds are at most squared if we make separate copies of the inputs to those AND-gates. Therefore, all of our results about majority-gates go through for formulas as well as for circuits. Our results about symmetric gates go through directly for formulas.

Our results also apply to circuits and formulas with threshold-gates having small weights. Some authors specify polynomial-bounded weights. A more general way of requiring small weights is to define the circuit size to be the number of wires plus the sum of all weights (then polynomial-size circuits automatically have polynomial-bounded weights). Then our results go through for threshold-gates in place of majority-gates, because we may convert such threshold-gates directly to rational functions with the same norm and degree bounds as in Lemma 3.4.

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